Docket No. AUS9-2000-0452-US1

CLAIMS:

What is claimed is:

1. A method for ensuring that data in a cached memory within a bus bridge is fresh, the method comprising:

monitoring signals from a host bridge for an indication of the state of the data within the cached memory; and

responsive to a determination that data in a portion of the cached memory is stale, clearing at least the portion of the cached memory containing the stale data.

2. The method as recited in claim 1, further comprising:

retrieving updated data corresponding to the stale data; and

storing the updated data in the cached memory.

3. The method as recited in claim 1, wherein the signals are sideband signals.

4. The method as recited in claim 1, wherein the signals indicate which pages within the cached memory are stale, and only those pages within the cached memory that are stale are discarded.

5. The method as recited in claim 1, wherein the step of clearing at least a portion of the cached memory comprises clearing the entire contents of the cached memory.

6. The method as recited in claim 1, wherein the bus bridge is a peripheral component interconnect to peripheral component interconnect bridge.

7. The method as recited in claim 1, wherein the host bridge is a peripheral component interconnect host bridge.

8. A method of providing data to an I/O adapter from a bus bridge, the method comprising:

receiving a request for data from the I/O adapter;

responsive to a determination that the requested data is contained within a cached memory, providing the requested data using the data in the cached memory.

9. The method as recited in claim 8, further comprising:

responsive to a determination that the requested data is not contained within the cached memory, retrieving the requested data from a system memory;

storing the data received from the system memory in the cached memory; and

providing at least a portion of the data received from the system memory to the requesting I/O adapter.

10. A peripheral component interconnect to peripheral component interconnect bridge, comprising:

an interface for sending and receiving data from a PCI host bridge;

an interface for sending and receiving data from an input/output adapter;

buffers for storing data;

an interface for receiving signals from the PCI host bridge indicating whether data in the buffers are stale; and

logic for clearing stale data from the buffers and retrieving fresh data from the PCI host bridge.

11. The peripheral component interconnect to peripheral component interconnect bridge as recited in claim 10, further comprising:

an interface for receiving signals from the PCI host bridge selecting one of a plurality of modes for handling stale data in the peripheral component interconnect to peripheral component interconnect bridge.

12. The peripheral component interconnect to peripheral component interconnect bridge as recited in claim 11, wherein the one of a plurality of modes comprises a mode in which all the data in the buffers is cleared in response to a signal received from the PCI host bridge indicating that at least some of the data in the buffers is stale.

13. The peripheral component interconnect to peripheral component interconnect bridge as recited in claim 11, wherein the one of a plurality of modes comprises a mode in which only the portion of the buffers for which the data has been determined to be stale are cleared.

14. The peripheral component interconnect to peripheral component interconnect bridge as recited in claim 11,

wherein the one of a plurality of modes comprises a mode in which the cached data is always refreshed prior to delivering requested data to the input/output adapter in response to a request for data.

15. A computer program product in a computer readable media for use in a data processing system for ensuring that data in a cached memory within a bus bridge is fresh, the computer program product comprising:

first instructions for monitoring signals from a host bridge for an indication of the state of the data within the cached memory; and

second instructions, responsive to a determination that data in a portion of the cached memory is stale, for clearing at least the portion of the cached memory containing the stale data.

16. The computer program product as recited in claim 15, further comprising:

third instructions for retrieving updated data corresponding to the stale data; and

fourth instructions for storing the updated data in the cached memory.

17. The computer program product as recited in claim 15, wherein the signals are sideband signals.

18. The computer program product as recited in claim 15, wherein the signals indicate which pages within the cached memory are stale, and only those pages within the cached memory that are stale are discarded.

19. The computer program product as recited in claim 5, wherein the second instructions comprise clearing the entire contents of the cached memory.

20. A computer program product in a computer readable media for use in a data processing system for providing data to an I/O adapter from a bus bridge, the computer program product comprising:

first instructions for receiving a request for data from the I/O adapter;

second instructions, responsive to a determination that the requested data is contained within a cached memory, for providing the requested data using the data in the cached memory.

21. The computer program product as recited in claim 20, further comprising:

third instructions, responsive to a determination that the requested data is not contained within the cached memory, for retrieving the requested data from a system memory;

fourth instructions for storing the data received from the system memory in the cached memory; and

fifth instructions for providing at least a portion of the data received from the system memory to the requesting I/O adapter.

22. A system for ensuring that data in a cached memory within a bus bridge is fresh, the system comprising:

first means for monitoring signals from a host

bridge for an indication of the state of the data within the cached memory; and

second means, responsive to a determination that data in a portion of the cached memory is stale, for clearing at least the portion of the cached memory containing the stale data.

23. The system as recited in claim 22, further comprising:

third means for retrieving updated data corresponding to the stale data; and

fourth means for storing the updated data in the cached memory.

24. The system as recited in claim 22, wherein the signals are sideband signals.

25. The system as recited in claim 22, wherein the signals indicate which pages within the cached memory are stale, and only those pages within the cached memory that are stale are discarded.

26. The system as recited in claim 5, wherein the second means comprise clearing the entire contents of the cached memory.

27. A system for providing data to an I/O adapter from a bus bridge, the system comprising:

first means for receiving a request for data from the I/O adapter;

second means, responsive to a determination that the

requested data is contained within a cached memory, for providing the requested data using the data in the cached memory.

28. The system as recited in claim 27, further comprising:

third means, responsive to a determination that the requested data is not contained within the cached memory, for retrieving the requested data from a system memory;

fourth means for storing the data received from the system memory in the cached memory; and

fifth means for providing at least a portion of the data received from the system memory to the requesting I/O adapter.